ABSTRACT OF THE DISCLOSURE

SEMIDIGITAL DELAY-LOCKED LOOP USING AN ANALOG-BASED FINITE STATE MACHINE

A low-power full-rate semidigital DLL architecture using an analog-based FSM (AFSM). The AFSM is a mixed-mode FSM in which analog integration is substituted for digital filtering, thus enabling a lower power implementation of the clock and data recovery function. An integrated voltage is converted to a digital code by an analog-to-digital converter (ADC), and the digital code is used either directly or after (low frequency) digital signal processing to control a a controllable delay element, such as, a phase rotator, for data edge tracking.